Surface mountable liquid crystal polymer package with vertical via transition compensating wire inductance up to V-band

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Abstract — **A high performance V-band surface mountable packaging structure has been proposed and demonstrated. We enabled the use of liquid crystal polymer (LCP) as a low-cost SMT millimeter-wave package. This package employed the wire bonding technique as the RF interconnect, and the vertical via as the vertical signal transition, despite it being meant for application up to V-band. The optimized vertical transition structure consisting of the vertical via and high-impedance transmission lines (TRLs) was designed to form a low-pass impedance matching network compensating for the parasitic inductance of the bonding wire. The overall packaging structure, including a bond wire, a vertical via and a solder joint, achieved excellent RF characteristics and a low insertion loss of less than 0.6 dB at 65 GHz. The adoption of widely used conventional technology such as a general printed circuit board (PCB) wiring process and a low-cost plastic substrate makes it possible to realize cost-effective millimeter-wave equipment.**

I. INTRODUCTION

To realize a consumer millimeter-wave radio system, the packaging and assembly costs must be reduced. Several ceramic-based packages for a surface mount in V-bands have been proposed [1-3]. Although these types of packages showed excellent RF performance, the cost issue still remained for the consumer equipment. Plastic packaging technologies can solve the cost issue, however the large mismatch of coefficient of thermal expansion (CTE) is still outstanding, and the poor accuracy of fabrication has prevented the achievement of high performance in the millimeter-wave region.

LCP is a promising material for electronics packaging substrate, much cheaper than Teflon® and LTCC. Additionally, its low dielectric constant is advantageous compared to the LTCC substrate for use in the high frequency range. Also, it has superior performance such as a low dissipation factor, low CTE, and desirable mechanical and chemical properties [4].

The wire bonding technology is widely applied at the interconnecting section between MMIC and its package circuit. Several techniques, such as attaching the distributed shunt capacitance and additional series inductive TRL to match the wire bonding section, have been widely used below 50 GHz [5], however the reflection caused by parasitic inductance has been shown to degrade RF characteristics seriously in the millimeter-wave region. Also, vertical vias have not been considered suitable for vertical transition structures in the millimeter-wave region because of their poor transmission characteristics [2]. The coupling slot circuit replacing vias have been reported above Ka-band [2,7], however, its passband width is limited. In addition, radiation losses occurring at solder joint sections degraded the transmission characteristics in the millimeter-wave range, and general PCB wiring rules limited the precise formation of circuit elements when using a plastic substrate.

In spite of these obstacles, the newly developed surface mountable package succeeded in achieving good RF performance. An equivalent circuit model derived from detailed analyses simplified the multipart circuit design to the prototype filter design. The vertical transition structure including the vertical via and adjacent lead lines was optimized to form a low-pass impedance network compensating for wire inductance over a wide frequency range. In addition, a newly proposed solder joint structure suppressed unwanted radiation loss. The introduction of the novel circuit design overcame the above-mentioned defects following traditional technologies still employed in the developed package.

It was confirmed from the measured results that even traditional technologies could sufficiently provide excellent package performance with very low insertion loss over a wide frequency range including V-band, by means of intelligent circuit design.

II. PACKAGE DESIGN

A. Package structure

A proposed RF transition structure in the developed package is illustrated in Fig.1. The whole transition structure consists mainly of three sections; a wire bonding section; a vertical via section; a solder joint section; and

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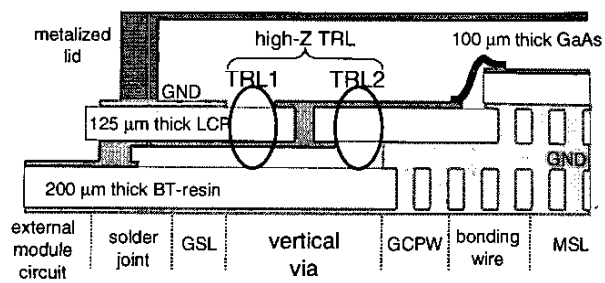

Fig. 1. RF transition structure in the developed package.

two interconnecting TRLs, one a grounded coplanar (GCPW) and one a grounded stripline (GSL).

The package is made of a 125 μm thick BIAC® LCP substrate laminated with 25 μm thick copper wiring layers on two sides of the substrate (Japan Gore-Tex Inc.). All designs were done on condition that the package would be installed on the motherboard circuit based on a 200 μm thick BT resin substrate. BIAC® has a dielectric constant of 3 and a dissipation factor of 0.003 (3 GHz). As LCP has been reported to have low dispersion characteristics [4], all 3-D full-wave analyses using Ansoft's HFSS were done without assuming any frequency dispersions up to 100 GHz. General PCB wiring rules were adopted for wiring patterning on both sides (line / space = 0.12 mm / 0.1 mm). Via holes are 280 μm in diameter and have via pads 600 μm in diameter.

A wedge bond aluminum wire with an effective length of 320 μm and a diameter of 25 μm was used as the interconnection. The wire bonding section attached to 35 Ω capacitive GCPW was expected to show a simulated maximum available gain (MAG) of –0.15 dB at 60 GHz. Its low dissipation characteristics suggested the potential of the wire bonding technology in V-band.

As illustrated in the figure, the vertical via section included lead lines with high characteristic impedances (TRL1 and TRL2). This section formed novel matching circuit compensating wire inductance over a wide frequency range up to V-band.

B. Equivalent circuit model as a low-pass matching network

An equivalent circuit model for each of the three sections was derived for the efficient optimization of the circuit, since a whole transition had many variable parameters. Accurate models consistent with all full-wave analyzed results with different structural parameters up to 80 GHz enabled us to distinguish the variable elements from the constant ones in the equivalent circuit. Also, it allowed us to quantify the variable range of the RF

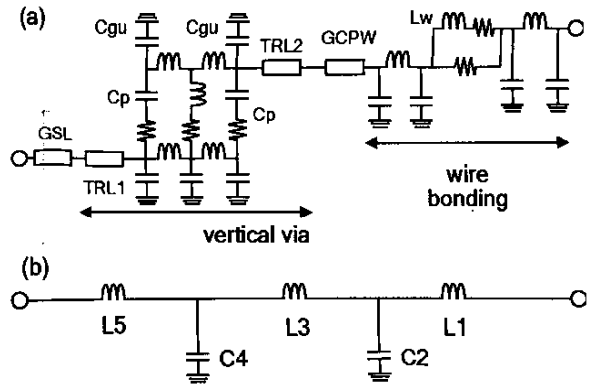

Fig. 2. (a) Equivalent circuit model of the whole transition structure excluding the solder joint section. (b) Simplified circuit model as low-pass matching network with five elements. Filter design theory requires L3 = 1.59L1 for Tchebyscheff filter response with 0.1 dB ripple.

characteristics of each section under general PCB rules. The developed model of the whole transition, excluding the solder joint section, is shown in Fig. 2 (a). Reducing C_{gu} and neglecting C_p simplified the total circuit to the low-pass prototype impedance matching network with five elements as shown in Fig. 2 (b), where C_{gu} is the grounded capacitance at the upper via pad and C_p is the coupling capacitance between the via pads. Here the five elements are L_w, the parasitic wire inductance, capacitive GCPW, the inductive TRL2, grounded capacitance at the bottom via pad, and the inductive TRL1.

Based on the basic theory of the filter design described in [6], an inductive element L1 requires a larger value for L3 to compensate. However L1 generated by the bonding wire was so large that the simulated reflection magnitude of the wire bonding section reached 0.43 at 60 GHz even after attaching to 35 Ω capacitive GCPW. Since TRLs with characteristic impedances lower than 80Ω have

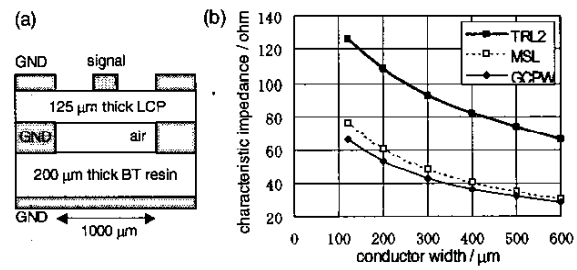

Fig. 3. (a) Cross sectional view of TRL2. (b) Calculated characteristic impedance of TRL2 as a function of conductor width. Also, the characteristic impedances of MSL and GCPW on 125 μm thick LCP substrate are shown.

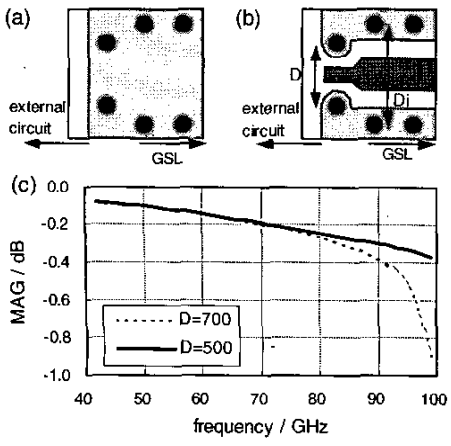

Fig. 4. Wiring patterns adopted to suppress unwanted radiation at the solder joint section. (a) pattern on LCP top surface, (b) pattern on LCP bottom surface with D=500 μm and Di=700 μm. Also in (c), simulated maximum available gain at the solder joint sections with D=500 μm and Di=700 μm (solid), and D=Di=700 μm (dotted) are shown.

never generated a high reflection of such magnitude, and established the conjugate matching conditions to the wire bonding section. Thus the most important feature in the design was setting the impedance of TRL2 to very high for generating a large inductance.

In order to achieve a high-impedance line in the structure, we used the lead line, TRL2 in the vertical via section as the part of the matching network positively. The removal of the ground patterns around the via pads effectively enhanced the characteristic impedance of TRL2 as illustrated in Fig. 3 (a). High impedance of about 130 Ω can be achieved at TRL2 under general PCB wiring rules, although conventional TRLs such as micro stripline (MSL) or GCPW structure on the same substrate cannot reach 80 Ω at their upper limit, as indicated in Fig. 3 (b). Also, this inductive performance can be insensitive to the variation of the vertical via forming, although the vertical transmission structure formed by signal vias and surrounding grounded vias could be affected by the variation of the via forming.

Adjusting the size of the bottom via pad from the theoretical required shunt capacitance, and setting the performance of TRL1 to inductive again, completed the low-pass network design.

C. Suppression of radiation loss at the solder joint section

Although several attempts such as the introduction of side via holes at the interface have been reported to

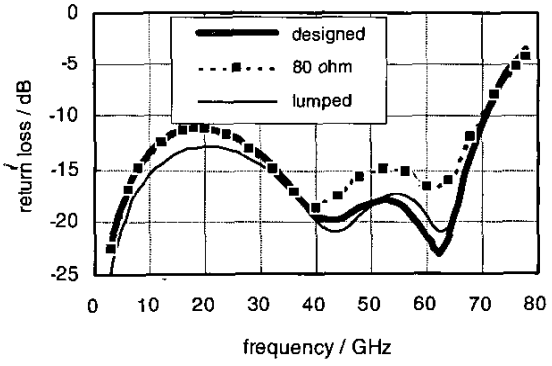

Fig. 5. Comparison of simulated reflection characteristics. A thick line indicates the full-wave analyzed performance of the developed package. A dotted line indicates optimized results of circuit simulation with ideal 80 Ω TRLs at TRL1 and TRL2. A thin line indicates that with lumped inductances at TRL1 and TRL2.

suppress unwanted radiation resonance in the LTCC package design [1], the low dielectric constant of LCP didn't bring any degradation of transmission characteristics up to 70 GHz without a special structure.

Fig. 4 illustrates the adopted wiring patterns at the solder joint section. For higher band applications above 70 GHz, the closer arrangement of grounded vias nearest to the interface was attempted. As compared to the conventional arrangement keeping between them, the distance D, the same as that of the inside region, Di, the closer arrangement, reduced the radiation loss at the solder joint section, and as indicated simulated MAG characteristics in Fig. 4 (c). No degradation in MAG characteristics below 95 GHz proved the advantage of low dielectric constant material for the package substrate application, and excellent simulated return losses better than –25 dB were obtained up to 80 GHz.

Fully analyzed characteristics of the whole transition after optimization are shown in Fig. 5 as a thick line. Slight degradation of return characteristics below 30 GHz was due to C_p, coupling capacitances between the via pads, and C_{gu}, grounded capacitances at the upper pad lowered its cutoff frequency. However, the designed characteristics achieved lower reflection than the optimized results assuming ideal 80 Ω TRLs at TRL1 and TRL2 in the circuit simulation. Also, the correspondence of bandwidth with a low reflection between the developed design and the lumped circuit simulation assuming lumped inductances at TRL1 and TRL2 is displayed in the figure. It proves the effectiveness of placing high-impedance TRLs in the structure.

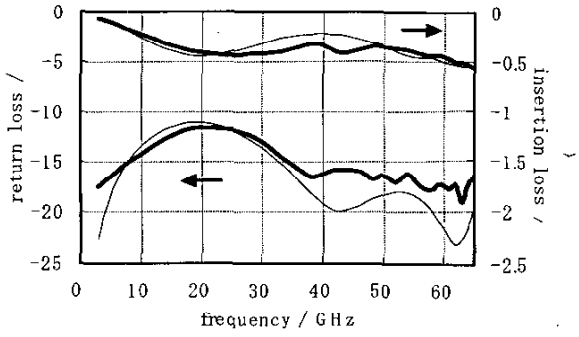

Fig. 6. Measured and simulated results of the developed package. The thick lines denote the measurement result and the thin lines denote the simulated result.

III. MEASUREMENTS

In order to validate our design concepts, 50 Ω Al_2O_3 MSL passive test chips with different line lengths were mounted on the optimized structures. Total circuit area per whole transition was 2.39 X 2.2 mm^2. The measurement system was calibrated using 2-port TRL calibration standards fabricated on motherboards. The data of a single transition were extracted from the measured data with different MSL lengths, since the measured data were for two ports, and interconnect MSL and motherboard circuits with a length of 1.2mm at each port. In Fig. 6, the calculated results with a single transition are plotted up to 65 GHz. The S-parameters demonstrate a whole transition is useful below 65 GHz, with a maximum insertion loss less than 0.6 dB. It should be noted that this value includes the wire loss, and the transmission intensity of -0.6 dB was nearly identical to the sum of the simulated MAGs of each section. Excellent return loss, better than 15 dB was achieved from 35 GHz to 65 GHz in spite of the insufficient accuracy of the fabrication which narrowed the passband width and degraded the return characteristics at the passband. The absence of sudden degradation in performance proved the usage of LCP in the millimeter-wave range, and validated the little dispersion assumed in all simulations. Also, the small differences between the simulated results and the measured results validated our approach.

IV. CONCLUSION

A V-band surface mountable LCP package has been developed. In the developed package, conventional wire bonding technology for MMIC interconnects and a vertical via transition structure for vertical signal transmission were used. The whole transition design intended to compensate wire inductance resulted in a low-pass prototype matching network design by fine-tuning lead lines in the vertical via transition as very high-impedance TRLs. Also, a newly proposed simple arrangement of the grounded vias at the solder joint section suppressed radiation loss. The measured results of mounting 50 Ω MSL test chips indicate that this package and design technology are promising for low-cost millimeter-wave equipment.

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